



## Hardware Design Verification: Simulation and Formal Method-Based Approaches

By William K. Lam

Pearson Education (US), United States, 2008. Paperback. Book Condition: New. 234 x 176 mm. Language: English . Brand New Book. The Practical, Start-to-Finish Guide to Modern Digital Design Verification As digital logic designs grow larger and more complex, functional verification has become the number one bottleneck in the design process. Reducing verification time is crucial to project success, yet many practicing engineers have had little formal training in verification, and little exposure to the newest solutions. Hardware Design Verification systematically presents today's most valuable simulation-based and formal verification techniques, helping test and design engineers choose the best approach for each project, quickly gain confidence in their designs, and move into fabrication far more rapidly. College students will find that coverage of verification principles and common industry practices will help them prepare for jobs as future verification engineers. Author William K. Lam, one of the world's leading experts in design verification, is a recent winner of the Chairman's Award for Innovation, Sun Microsystems most prestigious technical achievement award. Drawing on his wide-ranging experience, he introduces the foundational principles of verification, presents traditional techniques that have survived the test of time, and introduces emerging techniques for today's most...



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Design verification Process: Verification testing can be defined as a method of conf. Design Verification is a method to confirm if the output of a designed software product meets the input specifications by examining and providing evidence. The goal of the design verification process during software development is ensuring that the designed software product is the same as specified. Design input is any physical and performance requirement that is used as the basis for designing purpose. Design output is the result of each design phase and at the end of total design effort. The final design output is a basis for device master record. Difference between Design Verification and V SoC Design Verification. Using pre-defined and pre-verified building block can effectively reduce the productivity gap. Block (IP) based design approach Platform based design approach. But 60 % to 80 % of design effort is now dedicated to verification. Simulation-Based Verification. Still the primary approach for functional verification. In both gate-level and register-transfer level (RTL). Formal verification Use assistant hardware: Hardware accelerator ASIC emulator Rapid-prototyping(FPGA) Logic modeler

62. Hardware Design Verification: Simulation and Formal Method-Based Approaches. Learn More Buy. This chapter is from the book. The most prominent distinction between simulation-based verification and formal verification is that the former requires input vectors and the latter does not. The mind-set in simulation-based verification is first to generate input vectors and then to derive reference outputs. The thinking process is reversed in the formal verification process. The user starts out by stating what output behavior is desirable and then lets the formal checker prove or disprove it. Users do not concern themselves with input stimuli at all. In a way, the simulation-based methodology is input driven and the formal methodology is output driven. Hardware Design Verification: Simulation and Formal. Method-Based Approaches By William K. Lam, Sun Microsystems . Publisher: Prentice Hall PTR Pub Date: March 03, 2005 ISBN: 0-13-143347-4 Pages: 624. Table of Contents | Index. Formal verification is a relatively new technology and it complements simulation-based verification. I believe that to utilize a technology best, one must first be equipped with an in-depth understanding of the internal working principles of that technology. As a result, instead of just studying a verification tool's operations at the user level a topic better suited for user manualsthis book spends much time studying the fundamental principles of simulation and formal technology.

Hardware Design Verification by William K. Lam, March 3, 2005, Prentice Hall PTR edition, in English. Simulation and Formal Method-Based Approaches. First published in 2005. Edit. Hardware Design Verification: Simulation and Formal Method-Based Approaches (Prentice Hall Modern Semiconductor Design Series: PH Signal Integrity Library). This edition was published in March 3, 2005 by Prentice Hall PTR. Edition Notes. Out of print. Hardware Design Verification: Simulation and Formal Method-Based Approaches. William K. Lam. ©2005 |Prentice Hall | Out of print. engineers started out as designers and gradually transited to design verification. Unlike design techniques and methodologies, a broad range of verification. knowledge is loosely organized and informally acquired through hands-on. experiences. Formal Verification (where you are). Formal verification involves a mathematical proof to show that a design adheres to a property. Fully Depleted Silicon On Insulator (FD-SOI). FD-SOI is a semiconductor substrate material with lower current leakage compared than bulk CMOS. Verification language based on formal specification of behavior. IEEE 802.1-Higher Layer LAN Protocols. IEEE 802.1 is the standard and working group for higher layer LAN protocols. An approach in which machines are trained to favor basic behaviors and outcomes rather than explicitly programmed to do certain tasks. That results in optimization of both hardware and software to achieve a predictable range of results. Magnetoresistive RAM (MRAM).